AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS

1. (Original) A sequence control circuit comprising:

a program counter control section which decodes a sequence control instruction that is executed in the n-th cycle to output a program counter signal in the (n+1)th cycle as an instruction memory address for specifying a sequence control instruction that will be executed in the (n+1)th cycle; and

an instruction memory section which outputs said sequence control instruction executed in the (n+1)th cycle to said program counter control section in the (n+1)th cycle based on a program counter signal for specifying said sequence control instruction that is executed in the n-th cycle.

2. (Original) A sequence control circuit according to claim 1, wherein

said instruction memory section is accessed by said instruction memory address sent from said program counter control section, and is provided with a first storage area for storing a first sequence control instruction contained in the next line of the line specified by said instruction memory address and a second storage area for storing a second sequence control instruction contained in the line of the jump target of the instruction specified by said instruction memory address for each value of said instruction memory address, and

the circuit is further provided with a selector which selects either one of said first and second sequence control instructions that are read out from said instruction memory section in accordance with said instruction memory address, and

said program counter control section outputs not only said instruction memory address but also a selection signal whose level is determined by whether said sequence control instruction selected by said selector causes a jump operation to said selector.

3. (Original) A sequence control circuit according to claim 2, wherein when the selected sequence control instruction causes a jump operation, said program counter control section outputs a selection signal for directing said selector to select said second sequence control instruction, or otherwise when the selected sequence control instruction does not cause a jump operation, said program counter control section outputs a selection signal for directing said selector to select said first sequence control instruction.

4. (Original) A sequence control circuit according to claim 2, wherein

said instruction memory section includes first and second registers which hold said first and second sequence control instructions that are read from said first and second storage areas, respectively, and

said selector selects either one of outputs from said first and second registers in accordance with said selection signal.

5. (Original) A sequence control circuit according to claim 2, wherein said program counter control section includes a third register which holds said program counter signal

for specifying a sequence control instruction that will be executed in the (n+1)th cycle, and a fourth register which holds said selection signal.

6. (Original) A sequence control circuit according to claim 2, wherein said instruction memory section includes a first register which holds the sequence control instruction selected by said selector to output that to said program counter control section.

7. (Original) A sequence control circuit according to claim 2, wherein said program counter control section includes a second register which holds said program counter control signal for specifying the sequence control instruction that will be executed in said (n+1)th cycle, and directly outputs said selection signal to said selector.

8. (Original) A sequence control circuit according to claim 1, wherein the circuit is installed in a semiconductor testing apparatus which generates test patterns for testing a semiconductor device based on said instruction memory address.

9. (Currently Amended) A semiconductor testing apparatus comprising:

a pattern memory which stores pattern generating instructions for testing a semiconductor device;

a sequence control circuit ~~according to claim 1~~ which supplies an ~~said~~ instruction memory address to said pattern memory in order to control the output sequence of the pattern generating instructions that are read out from said pattern memory;

a pattern generating circuit which generates test patterns supplied to said semiconductor device and expectation patterns in accordance with said pattern generating instructions that are output from said pattern memory; and

a determination circuit which determines the quality of said semiconductor device based on said expectation patterns and signals that are sent from said semiconductor device in accordance with said test patterns,

wherein said sequence control circuit comprising:

a program counter control section which decodes a sequence control instruction that is executed in the n-th cycle to output a program counter signal in the (n+1)th cycle as said instruction memory address for specifying a sequence control instruction that will be executed in the (n+1)th cycle; and

an instruction memory section which outputs said sequence control instruction executed in the (n+1)th cycle to said program counter control section in the (n+1)th cycle based on a program counter signal for specifying said sequence control instruction that is executed in the n-th cycle.